ABSTRACT

0033 A method for forming an improved gate stack structure having improved electrical properties in a gate structure forming process A method for forming a high dielectric constant gate structure including providing a silicon substrate comprising exposed surface portions; forming an interfacial layer over the exposed surface portions having a thickness of less than about 10 Angstroms; forming a high dielectric constant metal oxide layer over the interfacial layer having a dielectric constant of greater than about 10; forming a barrier layer over the high dielectric constant metal oxide layer; forming an electrode layer over the barrier layer; and, etching according to an etching pattern through a thickness of the electrode layer, barrier layer, high dielectric constant material layer, and the interfacial layer to form a high dielectric constant gate structure.